

## CLAIMS

What is claimed is.

- 1 1. A process comprising:
  - 2 pressing an electrical bump against a film, wherein the electrical bump is
  - 3 disposed on a substrate; and
  - 4 forming a stress-compensation layer against the electrical bump, the
  - 5 substrate, and the film.
- 1 2. The process of claim 1, further including removing the film.
- 1 3. The process of claim 1, wherein removing the film at least partially exposes  
2 the electrical bump.
- 1 4. The process of claim 1, wherein pressing an electrical bump against a film  
2 includes embedding the electrical bump in the film in a range from about 5%  
3 embedded to about 95% embedded.
- 1 5. The process of claim 1, wherein forming a stress-compensation layer  
2 includes a process selected from capillary underfill, vacuum-assisted capillary  
3 underfill, positive-pressure assisted capillary underfill, and injection molding  
4 underfill.
- 1 6. The process of claim 1, wherein forming a stress-compensation layer  
2 includes a process of forming a particulate-containing stress-compensation layer.
- 1 7. The process of claim 1, further including curing the stress-compensation  
2 layer, selected from ultraviolet curing, microwave curing, thermal curing, chemical  
3 curing, timed curing, and combinations thereof.

1       8.     The process of claim 1, further including:  
2           curing the stress-compensation layer; and  
3           coupling the electrical bump with an electrical contact.

1       9.     The process of claim 1, further including:  
2           curing the stress-compensation layer; and  
3           coupling the electrical bump with an electrical contact, wherein curing the  
4           stress-compensation layer follows coupling the electrical bump.

1       10.    A process comprising:  
2           pressing an electrical bump in a ball grid array disposed on a substrate  
3           against a compressible film under conditions to at least partially embed the electrical  
4           bump into the compressible film;  
5           forming a stress-compensation layer between the substrate and the  
6           compressible film; and  
7           removing the compressible film.

1       11.    The process of claim 10, further including curing the stress-compensation  
2           layer.

1       12.    The process of claim 10, further including curing the stress-compensation  
2           layer, selected from ultraviolet curing, microwave curing, thermal curing, chemical  
3           curing, timed curing, and combinations thereof.

1       13.    The process of claim 10, wherein pressing an electrical bump includes  
2           embedding the electrical bump in the compressible film in a range from about 10%  
3           embedded to about 90% embedded.

1       14.    The process of claim 10, wherein forming a stress-compensation layer  
2           includes a process selected from capillary underfill, vacuum-assisted capillary

3 underfill, positive-pressure assisted capillary underfill, and injection molding  
4 compound underfill.

1 15. The process of claim 10, wherein forming a stress-compensation layer  
2 includes a process selected from capillary underfill, vacuum-assisted capillary  
3 underfill, positive-pressure assisted capillary underfill, and injection molding  
4 compound underfill, the process further including:  
5       curing the stress-compensation layer, selected from ultraviolet curing,  
6 microwave curing, thermal curing, chemical curing, timed curing, and combinations  
7 thereof.

1 16. The process of claim 10, wherein forming a stress-compensation layer  
2 includes a process of forming a particulate-containing stress-compensation layer.

1 17. An article comprising:  
2       a substrate including an upper surface;  
3       an electrical bump disposed on the upper surface; and  
4       a stress-compensation layer disposed on the upper surface, wherein the  
5 electrical bump is embedded in the stress-compensation layer, wherein the stress-  
6 compensation layer includes a surface profile characteristic of an imposed  
7 compressible film.

1 18. The article of claim 17, wherein the stress-compensation layer includes an  
2 underfill material selected from capillary underfill material, vacuum-assisted  
3 capillary underfill material, positive-pressure assisted capillary underfill material,  
4 and injection molding compound underfill material.

1 19. The article of claim 17, wherein the stress-compensation layer includes an  
2 underfill material, and wherein the underfill material includes a filler particulate.

1    20.    The article of claim 17, wherein the substrate is selected from a  
2    semiconductive device and a mounting substrate.

1    21.    A computing system comprising:  
2            a substrate including an upper surface;  
3            an electrical bump disposed on the upper surface;  
4            a stress-compensation layer disposed on the upper surface, wherein the  
5    electrical bump is embedded in the stress-compensation layer, wherein the stress-  
6    compensation layer includes a surface profile characteristic of an imposed  
7    compressible film; and  
8            at least one of an input device and an output device.

1    22.    The computing system of claim 21, wherein the substrate includes a  
2    microelectronic die.

1    23.    The computing system of claim 21, wherein the substrate includes a  
2    mounting substrate and further including a microelectronic die disposed on the  
3    mounting substrate on a die side thereof, and wherein the electrical bump is  
4    disposed opposite on a board side thereof.

1    24.    The computing system of claim 21, wherein the computing system is  
2    disposed in one of a computer, a wireless communicator, a hand-held device, an  
3    automobile, a locomotive, an aircraft, a watercraft, and a spacecraft.

1    25.    The computing system of claim 21, further including a microelectronic die,  
2    wherein the microelectronic die is selected from a data storage device, a digital  
3    signal processor, a micro controller, an application specific integrated circuit, and a  
4    microprocessor.

1       26.   A computing system comprising:  
2            a substrate including an upper surface;  
3            an electrical bump disposed on the upper surface;  
4            a stress-compensation layer disposed on the upper surface, wherein the  
5        electrical bump is embedded in the stress-compensation layer, wherein the stress-  
6        compensation layer includes a surface profile characteristic of an imposed  
7        compressible film;  
8            at least one of an input device and an output device; and  
9            a housing, wherein the housing encloses the stress-compensation layer.

1       27.   The computing system of claim 26, wherein the substrate includes a  
2        microelectronic die.

1       28.   The computing system of claim 26, wherein the substrate includes a  
2        mounting substrate and further including a microelectronic die disposed on the  
3        mounting substrate on a die side thereof, and wherein the electrical bump is  
4        disposed opposite on a board side thereof.

1       29.   The computing system of claim 26, wherein the computing system is  
2        disposed in one of a computer, a wireless communicator, a hand-held device, an  
3        automobile, a locomotive, an aircraft, a watercraft, and a spacecraft.

1       30.   The computing system of claim 26, further including a microelectronic die,  
2        wherein the microelectronic die is selected from a data storage device, a digital  
3        signal processor, a micro controller, an application specific integrated circuit, and a  
4        microprocessor.